

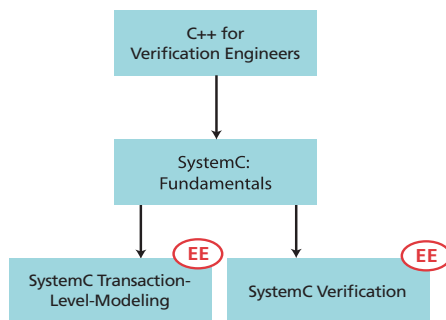
Tcl Scripting for EDA

This course highlights why Tcl is the leading scripting language for a wide variety of integration application needs. Whether you need to build a powerful GUI, embed Tcl in your application, create a multi-threaded application, or develop a cross-platform program, Tcl is your best choice.

SYSTEM C

C++ for Verification Engineers

C++ has become the leading language in the software engineering world. Its uses range from the creation of simple terminal-based applications all the way to large operating systems implementations. In the context of hardware engineering, C++ has historically been used for system-level modeling as well as verification. This course will cover the use of C++ and object-oriented programming from a hardware modeling perspective, focusing on the use of file operations, data processing, and the standard template library.



EE Advance with Engineer Explorer Series, designed for more experienced users

SystemC Fundamentals

This course covers the three main aspects of the SystemC® library: structural modeling, behavioral modeling, and debugging features. Throughout the laboratories, students will be asked to create register-transfer SystemC models, user-defined interfaces and channels, and data introspection functionalities. The laboratories can be performed using either the Cadence Incisive® simulator or the Open SystemC Initiative (OSCI®) reference simulator.

SystemC Transaction-Level Modeling

This is an Engineer Explorer series course designed around more advanced topics. Esperan's System-Level Modeling with TLM 2.0 course builds on your knowledge of the SystemC language, covering the newly provided APIs

and the modeling methods used to implement both the approximately-timed and loosely-timed transaction-level models (TLMs).

The course will discuss the benefits and issues encountered with TLMs such as refinement, standardised data types, and communication protocols. The course breaks in three main sections: the interfaces and channels section offers a detailed study of the available building components for TLM descriptions; the loosely-timed section and the approximately-timed sections explore design methods as well as practical examples of using TLMs.

SystemC Verification Libraries

This is an Engineer Explorer series course designed around more advanced topics and exploration of the SystemC language. Students will learn to architecture advanced and reusable transaction-level verification environments using the powerful specialized constructs included in the SystemC verification library such as constrained randomization, data introspection, and transaction recording.

SYSTEM VERILOG

SystemVerilog Design and Verification

The SystemVerilog course gives you an in-depth introduction to the main enhancements that SystemVerilog offers, discussing the benefits and issues with the new features and demonstrating how design and verification is more efficient and effective when using SystemVerilog constructs.

SystemVerilog Advanced Verification using OVM

The Open Verification Methodology (OVM) is the first open, interoperable, and proven verification reuse methodology for SystemVerilog. Based on the IEEE 1800 SystemVerilog standard, the OVM supports design and verification engineers developing advanced verification environments with higher levels of integration and portability of verification IP. This five-day course describes the background to the OVM, defines the standard, and explores how to use the OVM to develop powerful, reusable, and robust verification environments..

SystemVerilog Assertions (SVA)

This course gives you an in-depth introduction to SVA, along with guidelines

and methodologies to help you create, manage, and debug effective assertions for complex design properties. The two-day course is packed full of examples, case studies, and hands-on lab exercises to demonstrate real-life applications of SVA. The course examines different approaches to coding assertions, including workarounds for the restricted language support of some tools.

SystemVerilog Advanced SVA and Formal Verification

This course builds upon our SystemVerilog Assertions course to demonstrate advanced SVA features and introduce a methodology for using SVA in both formal verification and simulation. This course may be taken standalone by those with existing SVA knowledge, or as an add-on to the SystemVerilog Assertions course.

HDL VERIFICATION

Verification with PSL

This two-day course gives you an in-depth introduction to the language, along with guidelines and methodologies to help you create, manage, and debug effective assertions for complex design protocols.

The course is packed full of examples and case studies to demonstrate real-life applications of the language. We also examine different approaches to coding assertions, including workarounds for the restricted language support of some tools. To acquire further expertise on PSL, we encourage you to attend a third day on Advanced PSL and Formal Verification.

Advanced PSL and Formal Verification

This course builds upon the two-day Verification with PSL course to show advanced PSL features and introduce a methodology for using PSL in both formal verification and simulation. This course may be taken standalone by those with existing PSL knowledge, or as an add-on to the Verification with PSL course.

If you have any questions or would like assistance in selecting a program tailored to your needs and interests, please contact us at

eur_training@cadence.com

Education Services EMEA