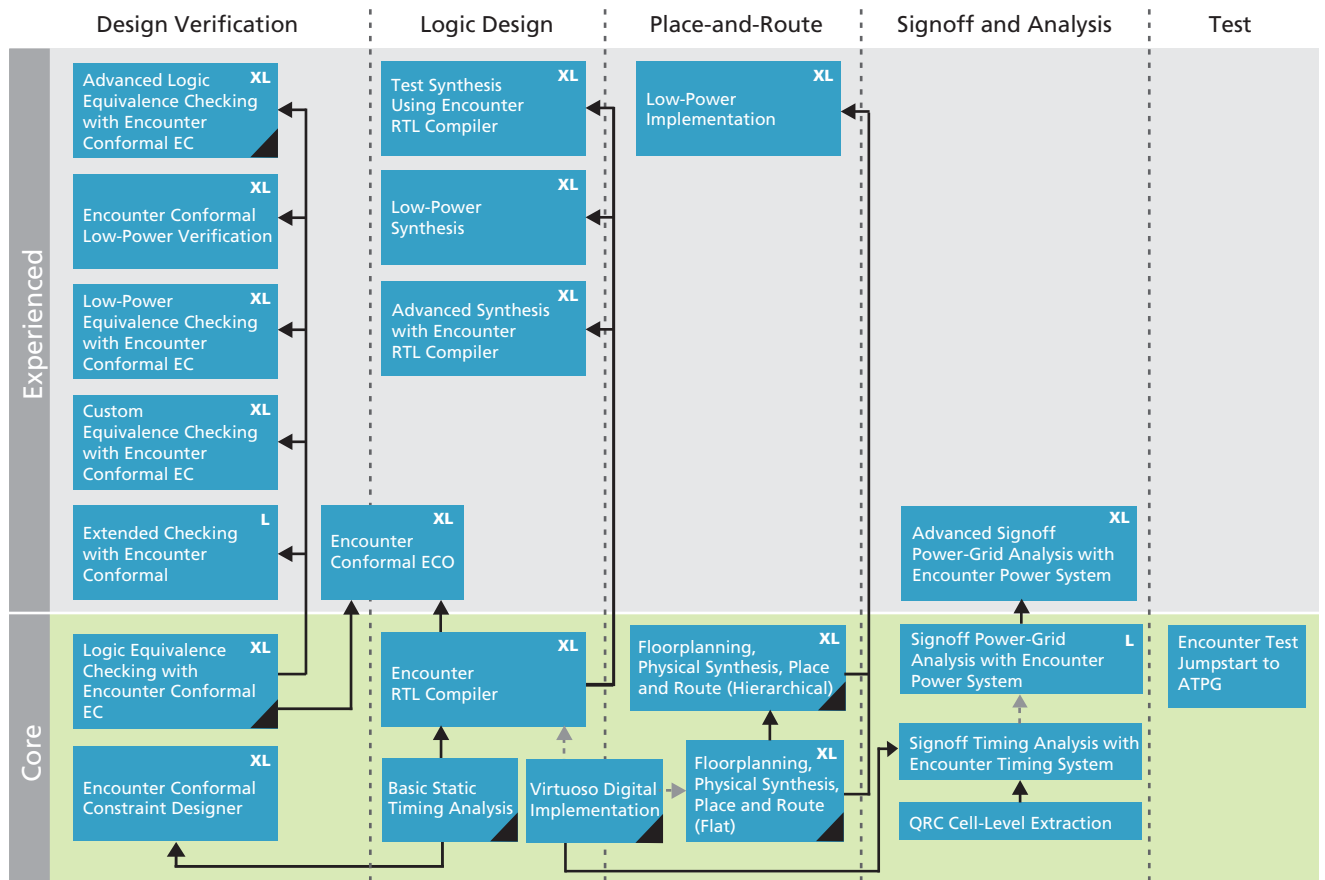


## EMEA TRAINING

### A direct path to increased productivity

Cadence® Education Services can help you get the most out of your investment. With its innovative and hands-on course content, state-of-the-art training centers, 200+ certified instructors, and a variety of learning modes (instructor-led, self-paced, and virtual), Cadence Education Services helps you become proficient with Cadence software, EDA languages, and design methodologies—quickly and cost-effectively.

### DIGITAL DESIGN AND ENCOUNTER TECHNOLOGY



▲ Also available as an Internet Learning Series course.  
 Course titles may vary. Please refer to your regional catalog for exact titles & course datasheets.  
 L, XL, GXL Denotes tiers of Cadence products

#### FORMAL VERIFICATION

##### LOGIC EQUIVALENCE CHECKING WITH ENCOUNTER CONFORMAL EC

In this course, you use the Encounter® Conformal® Equivalence Checker to perform functional verification. You learn the basic flow of equivalence checking and how to run hierarchical comparison of designs. The lab exercises follow major

topics and are designed to be directly applicable in design and design verification. After completing this course, you will be able to set up and verify your designs, analyze the results, and debug failing results.

##### ADVANCED LOGIC EQUIVALENCE CHECKING WITH ENCOUNTER CONFORMAL EC

In this Advance with Engineer Explorer course, you learn

systematic procedures for diagnosing the nonequivalences caused by setup, modeling, and mapping issues. You learn techniques to resolve the nonequivalences. You also identify, analyze, and resolve the aborts during design comparison. The labs help you master the recommended analysis techniques and use the Encounter Conformal Equivalence Checker (EC) to debug common problems.

## ENCOUNTER CONFORMAL ECO V8.1

Cadence® Encounter® Conformal® ECO Designer combines logic equivalence checking (for the most complex SoC and datapath-intensive designs) with functional ECO analysis and generation, design netlist modification, clock domain synchronization, and semantics checks. This course provides an in-depth look at the software along with hands-on experience required to use the tool. With a complete ECO solution that spans different parts of the RTL-to-GDSII flow, design teams benefit from automation, predictability, and the highest quality ECOs.

## RTL SYNTHESIS

### ENCOUNTER RTL COMPILER

In this course, you will explore the features of the Cadence® Encounter® RTL Compiler with global synthesis technology. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, design for low power, and interface with other tools.

### ADVANCED SYNTHESIS WITH ENCOUNTER RTL COMPILER

This is an Engineer Explorer course for designers that need a more detailed understanding of and already have experience in Encounter RTL Compiler. In this course, you use Encounter® RTL Compiler global synthesis to debug problems in the synthesis of complex designs when optimizing for timing, area, and power. You also learn to use the synthesis flow to achieve better quality of results for the place-and-route tools.

### TEST SYNTHESIS USING ENCOUNTER RTL COMPILER

In this one day course, you learn to use Encounter® RTL Compiler to insert test structures in your design, synthesize for test, and connect scan chains.

## CHIP IMPLEMENTATION

### LOW-POWER IMPLEMENTATION - FRONT END / BACK END

In these Advance with Engineer Explorer Series courses, designers

familiar with digital implementation using the Encounter® platform explore and implement several low-power techniques to reduce both dynamic and leakage power during synthesis and design implementation. You run formal verification to ensure the functionality of the low-power design.

## SILICON VIRTUAL PROTOTYPING & PHYSICAL SYNTHESIS

### FLOORPLANNING, PHYSICAL SYNTHESIS, PLACE AND ROUTE (FLAT)

You will explore high-level design planning and implementation by using the SoC Encounter® XL software. Furthermore, we will show you several techniques for floorplanning and placement, while implementing timing closure strategies. You run the detail router to route a design, fix routing violations, and use timing and signal integrity options. Other topics in this course include extracting parasitics, creating clock trees, running delay calculation, and database access commands. You also explore wire editing, metal fill, ECO, and physical verification.

### FLOORPLANNING, PHYSICAL SYNTHESIS, PLACE AND ROUTE (HIERARCHICAL)

In this course, you explore the features of the SoC Encounter® software for creating and implementing a hierarchical design. You learn several techniques to floorplan your design, create partitions (hierarchical blocks), run place and route, and optimization (both at the block-level and top-level) to close timing. You will learn techniques to reduce the memory-size and run-time by using iLMs and Active Logic Reduction(ART) technology.

## TIMING & SIGNAL INTEGRITY ANALYSIS

### SIGNOFF TIMING ANALYSIS WITH ENCOUNTER TIMING SYSTEM

This is an Engineer Explorer course for designers familiar with Static Timing Analysis (STA). This course is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Encounter® Timing System. You analyze a design for static timing,

signal integrity with crosstalk coupling, and IR drop and multi-supply multi-voltage (MSMV) effects that are inherent in advanced process nodes with feature sizes 90 nm and below. This will ensure the highest probability of first silicon success.

## POWER ANALYSIS

### SIGNOFF POWER-GRID ANALYSIS WITH ENCOUNTER POWER SYSTEM

This is an Engineer Explorer course for designers that need a comprehensive and detailed understanding of power rail analysis for advanced processes. In the first day of the course, you run early rail analysis using SoC Encounter™ XL technology, and basic rail and IR-drop analysis using Encounter Power System. You create power-grid view libraries. You also run static and dynamic power-consumption analyses. In the second day of the course, you study more advanced power rail analysis, decapacitance optimization, the *common power format* (CPF), and power-up analysis.

### ADVANCED SIGNOFF POWER-GRID ANALYSIS WITH ENCOUNTER POWER SYSTEM

In this Engineer Explorer course, you learn advanced features of the Encounter® Power System including advanced library generation, Common Power Format (CPF) usage, power-up analysis, and thermal analysis.

If you have any questions or would like assistance in selecting a program tailored to your needs and interests, please contact us at

[eur\\_training@cadence.com](mailto:eur_training@cadence.com)

Education Services EMEA