

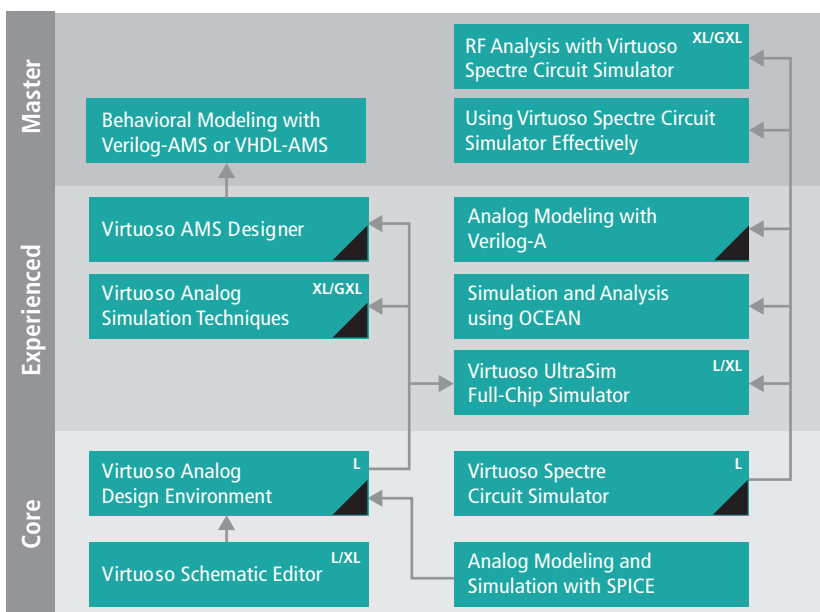


## EMEA TRAINING

### A Direct Path to Increased Productivity

Cadence® Education Services can help you get the most out of your investment. With its innovative and hands-on course content, state-of-the-art training centers, 200+ certified instructors, and variety of learning modes (instructor-led, self-paced, and virtual), Cadence Education Services helps you become proficient with Cadence software, EDA languages, and design methodologies—quickly and cost-effectively.

#### VIRTUOSO ANALOG/MIXED-SIGNAL COURSES



▲ Also available as an Internet Learning Series course. L/XL/GXL denotes tiers of Cadence products.

#### Virtuoso Analog Design Environment

This course introduces the Virtuoso Analog Design Environment L for setting up and controlling analog and mixed-signal simulations. You will run simulations using Cadence analog simulators, such as Spectre®, Spectre Turbo, and UltraSim simulators, and be exposed to the power of our newest analog simulator, Virtuoso Accelerated Parallel Simulator. You will also run specialized simulations, such as device checking, DC match, and Virtuoso Analog VoltageStorm®/ Analog ElectronStorm® Options, and be introduced to the OCEAN scripting language.

#### Virtuoso Analog Simulation Techniques

In this course, you will learn advanced simulation techniques such as multiple sweeps, corners, Monte Carlo, designing to specifications, and optimization through component parameterization.

#### Using Virtuoso Spectre Simulator Effectively

This advanced Engineer Explorer course offers an in-depth look at the workings of the Spectre Circuit Simulator. You will learn the DC and AC analysis algorithms used by the simulator and the options and properties that affect the simulation. You will also investigate Stability analysis and Discrete Fourier Transform (DFT).

#### RF Analysis with Virtuoso Spectre Simulator

This course explores applications of the Shooting Newton and Harmonic Balance engines used for RF analysis in the Spectre Circuit Simulator environment. You will learn to set up, simulate, and analyze RF applications more quickly and more efficiently running periodic steady state (PSS) analysis, small-signal analysis, and quasi-periodic steady state (QPSS) analysis.

#### Virtuoso UltraSim Full-Chip Simulator

In this course, you will learn to use the UltraSim Fast-SPICE simulator to run large transistor-based simulations, including an extensive set of checking commands, power analyses, and IR drop and electromigration tests.

#### Virtuoso AMS Designer

In this course, you will learn to run and debug large and complex mixed-signal, mixed-language simulations from both the command line and the GUI using Verilog, Verilog-A, Verilog-AMS, VHDL, VHDL-AMS, Virtuoso Schematic Editor, and Spectre and SPICE design blocks in mixed configurations.

#### Analog Modeling and Simulation with SPICE by Andrei Vladimirescu

This course will help circuit designers better understand semiconductor device modeling, with emphasis on deep-submicron (DSM) technology and the operation of a SPICE circuit simulator. The course will also address the different levels of modeling (structural and behavioral), the simulation controls available to the user, and new types of analysis such as steady-state that are particularly suited for RF design.

## Analog Modeling with Verilog-A

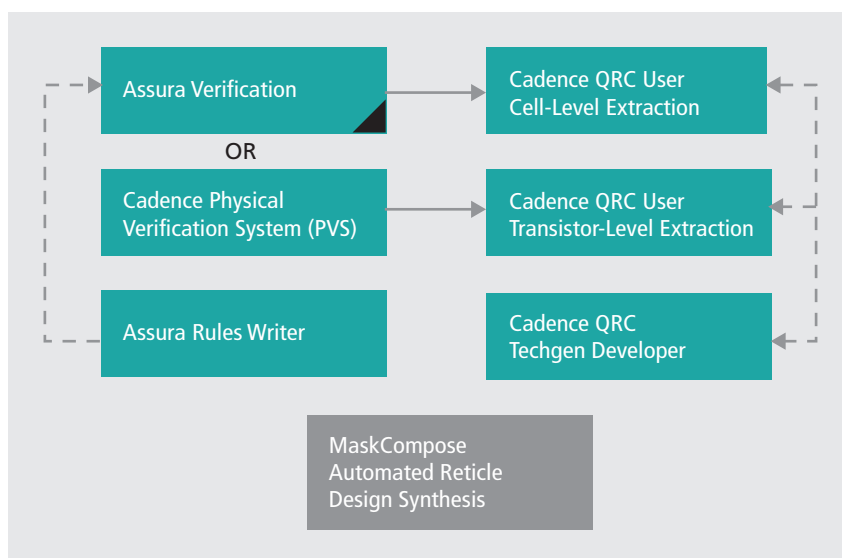
Verilog-A is a high-level language that uses modules to describe the structure and behavior of analog systems and their components. In this course, you will use the Virtuoso Analog Design Environment and Virtuoso Spectre Circuit Simulator to simulate analog circuits using Verilog-A models.

## Behavioral Modeling with Verilog-AMS or VHDL-AMS

These advanced Engineer Explorer courses provide an in-depth approach to writing realistic behavioral models of analog and mixed-signal design blocks and systems using the respective modeling language.

If you have any questions or would like assistance in selecting a program tailored to your needs and interests, please contact us at [eur\\_training@cadence.com](mailto:eur_training@cadence.com)  
Education Services EMEA

## DESIGN FOR MANUFACTURING COURSES



Also available as an Internet Learning Series course.

### Assura Rules Writer

This course provides complete application instructions for all aspects of physical verification. The techniques covered are applicable to all technologies and process types:

- CMOS
- Bipolar
- High/low voltage
- Memory
- Analog/mixed signal
- ASIC

### Assura Verification

This course covers aspects of using the Assura® DRC and Assura LVS tools for design rule checks, short location, and layout-versus-schematic checks. In labs, students will execute DRC and LVS, as well as debug error results.

### Cadence QRC Techgen Developer

This course provides an overview of parasitic extraction, showing you how to use existing RCX or QX technology files to create a technology file for the new Cadence QRC Extraction tool.

### Cadence QRC User Transistor-Level Extraction

In this transistor-level parasitic extraction course for analog and full-custom circuits, you will do multiple runs of layout-vs.-schematic checks and extraction to learn a representative array of options for extraction in preparation for simulation. You will then use the Virtuoso Analog Design Environment to run simulations on the schematic and compare the results to a simulation including the extracted parasitics.

### Cadence QRC User Cell-Level Extraction

In this one-day course, you will explore parasitic extraction for standard-cell logic blocks in digital designs. You will use Cadence QRC Extraction for basic extraction and advanced capacitance extraction. You will learn how to restart an extraction session in case of hardware failures or engineering change orders (ECOs). You will also extract metal fill effects using the virtual metal fill function.

### MaskCompose Automated Reticle Design Synthesis

In this course, you will learn to use MaskCompose Automated Reticle Design Synthesis for the following tasks:

- Generating a frame
- Preparing a fracture
- Creating jobdecks
- Preparing order forms
- Creating customized documentation
- Generating a shot map

### Cadence Physical Verification System (PVS)

This course will cover practical methods of running and debugging DRC, ERC, and LVS. Users will learn how to use the powerful and straightforward PVS debugging environment to locate errors and fix real problems in a quick turnaround time. The training includes lessons on antenna and density checking, fill generation, interactive short locator, HyperDebug, cross probing, Layout-XOR, schematic-vs.-schematic, integration with QuickView, and more. It will also introduce the PVL rules language.

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