

CADENCE TRAINING

CADENCE TRAINING BROCHURE

2010 - 2011



cādence[®]

Color Legend and Quick Access to Platform-Specific Training Courses

PCB AND PACKAGE DESIGN WITH ALLEGRO TECHNOLOGY	6
CUSTOM DESIGN WITH VIRTUOSO AND ASSURA TECHNOLOGY	8
DIGITAL DESIGN WITH ENCOUNTER TECHNOLOGY	10
DIGITAL VERIFICATION, LANGUAGES, AND METHODOLOGIES WITH INCISIVE TECHNOLOGY	12

Industry studies show that technology training results in a 20-30% productivity gain

“Virtual training is a necessity in today’s working environment. Cadence Virtual Training allows for teams located across the globe to take the same class simultaneously, without the cost or burden of traveling. More employees have the opportunity to take a variety of classes and the convenience of flexible class times. They still benefit from student-teacher interaction, as well as interaction among the students. IBM operates in a globally integrated environment that demands this kind of virtual education.”

Susan Benysh, Ph.D., PMP
IBM Corporation
Rochester, Minnesota, USA



A DIRECT PATH TO INCREASED PRODUCTIVITY

People are the most valuable resource for an organization, which makes it critical that they have the training required to perform their jobs effectively.

Cadence® Training offers a wide range of courses that give you the best possible return on your investment in EDA technologies.

By attending our training courses, Cadence will help you gain first-class knowledge and increased efficiencies on our tools, on languages and methodologies, and on flow optimization.

Cadence Training courses deliver real solutions that contribute to your success.

By attending a course, you will:

- Improve efficiency and boost your confidence in the tools
- Strengthen your skills in identifying and solving specific problems
- Increase the accuracy of your designs
- Enhance your in-house problem-solving skills
- Learn directly from the experts, with someone on-hand to help

DIMENSIONS OF TRAINING

Technology: What the tools do and how to access technology effectively

Methodology: Combining capabilities into a consistent and repeatable flow

Applicability: How to apply features, methodologies, and design skills to reach the desired goal

Product Technology

- In-depth tool training taught by tool experts
- Hands-on experience presented in the context of the target solution

Methodology

- Utilizes and teaches ready-to-use methodologies and flows that take advantage of advanced product technology and production-proven results

Applicability

- Includes training on design theory and techniques, taught by design engineers
- Leverages the practical design experience of the Cadence Services organization

Program Management and Delivery

- Delivered by a team of design and tool experts
- Highly focused programs targeting your specific needs

LEARNING OPTIONS

Cadence recognizes that everyone has different requirements. Whether your particular needs concern customized course content or a specific form of commercial agreement, Cadence provides a range of training formats for you to achieve your learning objectives:

Standard Training Courses

Developed with pre-defined sets of topics, Standard Training courses are offered at Cadence training facilities or can be delivered onsite at your facility.

Advance with Engineer Explorer (EE) Training

Designed for expert engineers, Advance with EE courses address specific and advanced functionalities to solve difficult technology challenges.

Tailored Training Courses

Course topics for Tailored Training are the same as those found in Standard Training or EE classes, but Tailored courses offer you the option to mix, add, or eliminate topics from one course or multiple courses.

Custom Training Courses

Custom Training provides you with maximum flexibility. Material is based on Standard course material, but you can request that only certain topics be covered or that new topics be added. You can also provide your own design or database to use in the labs.

Design Foundations Courses

These courses combine instruction on design theory, approaches, and practices with product, flow, and methodology training to help you develop all of the competencies required to be productive in a particular discipline or transition.

DELIVERY OPTIONS

Cadence also provides a range of delivery options to accommodate your learning style and travel budget:

Face-to-Face Courses

- Public courses at one of our training centers
- Private courses offered at the customer's site
- Tailored, Custom, or Advance with EE courses either at your site or at one of our training centers

Remote Instructor-Led Courses

- Virtual courses taught by a remote trainer from any location you choose, eliminating the need to travel

Online Courses Available 24x7

- Internet Learning Series (iLS) courses delivered over the web, allowing you to work at your own pace and in your own environment, 24x7

REGISTERING FOR A CADENCE TRAINING COURSE

Cadence Training staff can offer guidance in selecting a suitable training plan.

If you have questions or would like help in selecting your courses, contact the Cadence Training staff. We will be happy to help you select the most appropriate course to meet your needs and expectations.

General Terms, Conditions, and Cancellation Policy are published on each regional Cadence Training website at www.cadence.com/training.

TRAINING CENTERS

Most Cadence training centers are fully equipped with Windows and Linux workstations. Cadence promotes a comfortable studying environment, with rooms designed to facilitate learning and development.



REMOTE LEARNING OPTIONS

Two New Ways to Get Educated—Minus the Hassle, Expenses, and Travel Time

- Our **Internet Learning Series (iLS)** is comprised of self-paced courses delivered over the web that let you proceed at your own pace, anytime and anywhere. Our iLS courses include dynamic course content, downloadable labs, instructor notes, and bulletin boards.
- Our **virtual classrooms** are web-based environments that allow you to participate in live training events without having to travel. You can listen to lectures, participate in lab exercises, ask questions, and receive feedback just as you would in a conventional classroom, but you do it from the convenience of your desktop, or anywhere you have an Internet and phone connection.

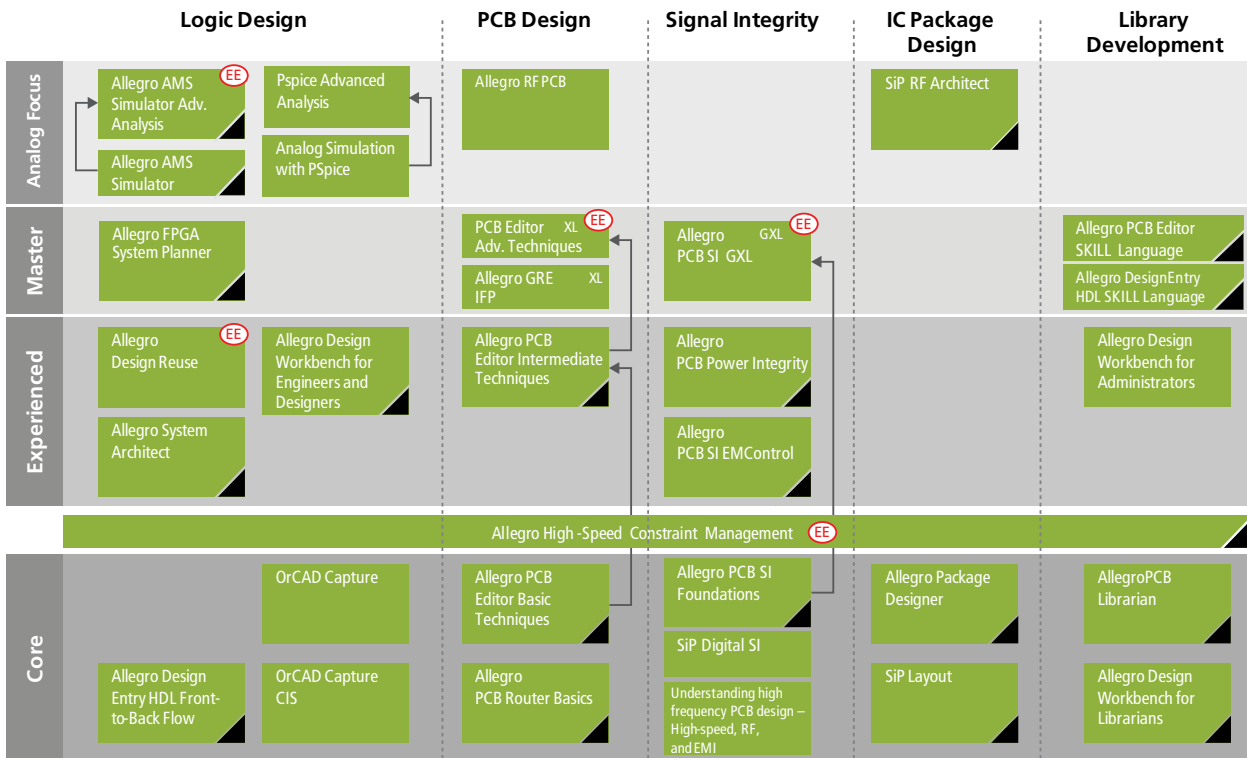


For the most up to date information on
Cadence training, please visit

www.cadence.com/training

PCB AND PACKAGE DESIGN, WITH ALLEGRO TECHNOLOGY

Learning Map



▲ Also available as an Internet Learning Series course. ^{EE} Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Some course titles may vary. Please refer to your regional catalog for exact titles & course datasheets.

Course Descriptions

Logic Design

Allegro® Design Entry HDL Front-to-Back Flow: This course teaches you how to use Design Entry HDL to create board-level schematic designs and demonstrate the integration between Design Entry HDL and other tools in the design flow, including the PCB Editor.

OrCAD Capture/OrCAD Capture CIS: This course covers the full range of front-end design processes, from setting up design templates to creating a netlist for board layout, as well as part management.

Allegro System Architect: The course introduces you to a new paradigm in design entry, making use of a spreadsheet- or table-based System Connectivity Manager tool.

Allegro Design Reuse: Design Reuse is the creation of a logical block and physical layout representing a standalone portion of a design. The logical and physical data is placed in a library for others to reuse.

Allegro Design Workbench for Engineers and Designers: The course begins with a brief overview of Allegro Design Workbench products. You are shown how to create a new project, search and add parts to your schematic using the component browser, take the design to layout, and backannotate.

Allegro FPGA System Planner: This course shows you how to define your FPGA system and synthesize the connections in your design. You generate a schematic and PCB Editor database so the FPGA I/O assignments can be optimized in the board environment.

Allegro AMS Simulator: The AMS Simulator class is a three-day course that starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the tool.

Allegro AMS Simulator Advanced Analysis: Focuses on library and design analysis-related issues of concern to the advanced user.

Analog Simulation with PSpice: This three-day course starts with the basics of entering a design for simulation and builds a solid foundation in the overall use of the tool.

PSpice Advanced Analysis: This class focuses on library, models, convergence and design analysis-related issues of concern to the advanced user.

PCB Design

Allegro PCB Editor Basic Techniques: This course covers all the necessary steps for designing a PCB, from loading logic and netlist data through producing manufacturing/NC output.

Allegro PCB Editor Intermediate Techniques: This course gives you a deeper understanding of the software and presents features and tips. Some of the items covered are exploration of high-speed design rules, creating areas in your design that require different routing rules, and generating test points. In the task-oriented labs, you use a combination of interactive and automatic tools.

Allegro PCB Editor Advanced Techniques: After completing the course, you will have a better understanding of the intricacies of the PCB Editor software and be able to optimize your PCB design environment to improve productivity and reduce time to market.

Allegro PCB Router: This course teaches you how to use the Allegro PCB Router and interactive wire editing tools.

Allegro RF PCB: In this course, you learn about various RF PCB front to back flows.

Allegro GRE IFP: The Global Route Environment (GRE) provides the technology and methodology to capture as well as adhere to a designer's intent. In the Allegro GRE Interconnect Flow Planning course, you apply this technology and methodology to convert your design intent into the final board design.

Signal Integrity

Allegro PCB SI Foundations: This course teaches you how to use the Allegro PCB SI tool to successfully develop and drive design rules for high-speed designs.

SiP Digital SI: In this course, you will use the SiP Digital SI XL tool to analyze the high-speed nets in a multi-chip module. You will also use the Topology Editor to extract topologies from the design for analysis, as well as create your own topologies to explore design technology tradeoffs.

Understanding High Frequency PCB Design – High Speed, RF and EMI: Part 1 of this two-part course applies basic physical principles to develop an understanding of the key issues of high-speed design, thereby ensuring a successful design for signal integrity. Part 2 of this two-part course builds seamlessly on the principles and practices established in Part 1, extending them to develop techniques for design and test at frequencies above 1 GHz for Gb/s serial transmission and for controlling the generation and propagation of EMI at the PCB level.

Allegro PCB SI EMControl: Allegro PCB SI EMControl helps you to detect problems by enabling you to repeatedly check your design against selected sets of EMC rules chosen by a user who has expertise in EMC.

Allegro PCB Power Integrity: This course provides a coherent methodology for the design and fabrication of power distribution systems (PDS) in high-speed printed circuit boards (PCB). Power distribution system design includes voltage regulator modules, decoupling capacitors, and power/ground planes.

Allegro PCB SI GXL: This course is intended to bring users up to speed on the technical aspects of Allegro PCB SI GXL.

IC Package Design

SiP Layout: This course takes you through a complete design flow of a System in Package (SiP) design, from defining the module outline through placing components; defining a netlist; placement; routing; and documentation and manufacturing output. The course covers the complete design flow for a flip-chip and wire-bonded stacked die module using the Cadence SiP Digital Layout software.

Allegro Package Designer: This course discusses the Allegro Package Designer system. It covers the design and specifications for manufacturing single-chip modules for single-, double-, or multi-layered analog and digital packages.

SiP RF Architect: This class shows the student how to use a design flow between the Cadence Virtuoso® design environment and the SiP Layout environment. It enables designers to create a single, system-level, circuit simulation-ready schematic for an RF/analog die, SiP substrate, and packaged and embedded discrete devices.

Library Development

Allegro PCB Librarian: In this course, you are introduced to the Allegro PCB Librarian product bundle, which includes the Library Explorer, the Part Developer, and PCB Editor. Next, you learn how to create a development and testing area for new Allegro Design Entry HDL (DE HDL) and PCB Editor parts. The rest of the class focuses on building and testing many different kinds of parts. Each part illustrates a particular concept or highlights a capability within the library tools.

Allegro Design Workbench for Librarians: The course begins with a brief overview of Allegro Design Workbench products. You will learn how to create a new project, new parts, new schematic models, and new footprint models. You will also be taken through an ECO flow to update an existing part.

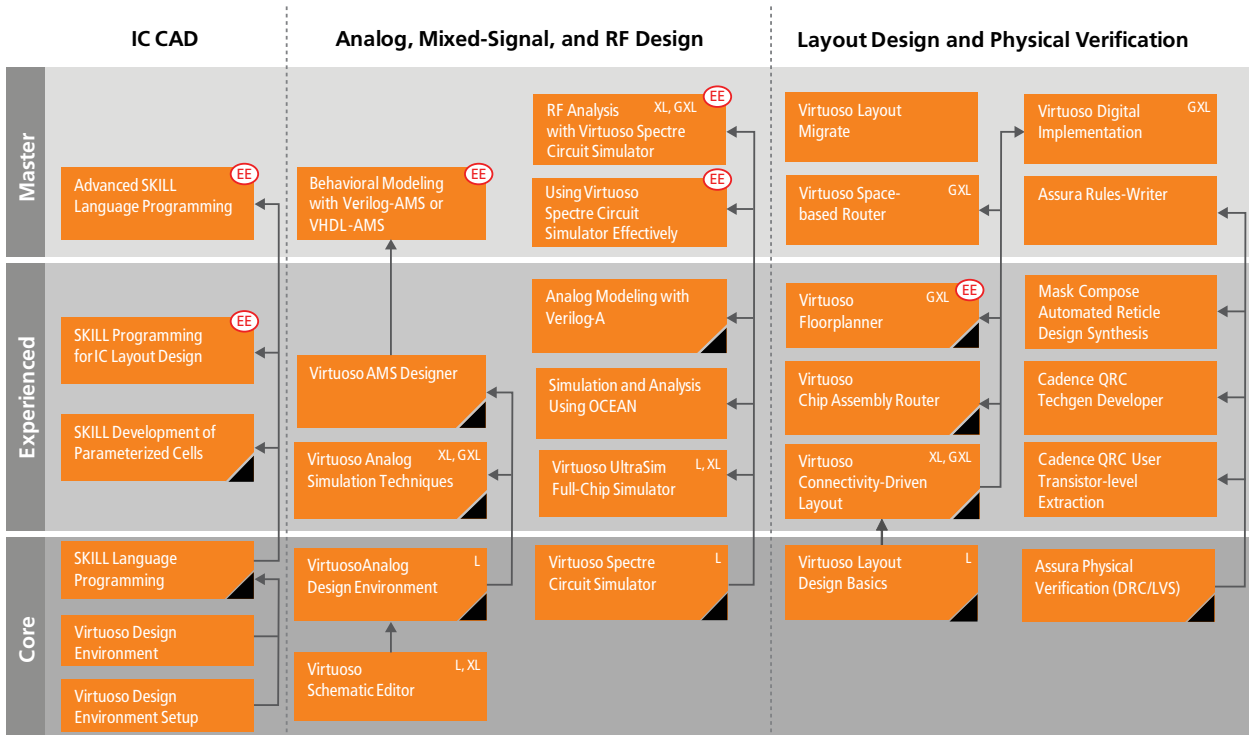
Allegro Design Workbench for Administrators: The Allegro Design Workbench for Administrators course is designed for users who will be responsible for updating and maintaining the Allegro Design Workbench environment and databases.

Allegro PCB Editor SKILL Language: The Allegro PCB Editor SKILL Programming Language course provides you with the basic knowledge required to begin writing useful commands and functions to customize and extend the functionality of the base PCB Editor and Advanced Package Designer (APD) tool set.

Allegro DE HDL SKILL Language: The Allegro Design Entry HDL SKILL Programming Language course provides you with the basic knowledge required to begin writing useful commands and functions to customize and extend the functionality of the base Design Entry HDL tool set.

CUSTOM DESIGN WITH VIRTUOSO AND ASSURA TECHNOLOGY

Learning Map



Also available as an Internet Learning Series course. (EE) Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Some course titles may vary. Please refer to your regional catalog for exact titles & course datasheets.

Course Descriptions

Analog Design

Virtuoso® Schematic Editor: In this course you learn how to create schematics, symbols, inherited connections, and attach constraints.

Virtuoso Analog Design Environment: In this course, you learn how to simulate analog circuits with a variety of simulators, featuring Spectre® and Spectre Turbo, apply parametric sweeps, re-simulate with extracted parasitics and check the conditions and devices in your designs including IR Drop and Electromigration.

Virtuoso Analog Simulation Techniques: In this course using ADE-XL/GXL, you learn advanced simulation techniques such as multiple sweeps, corners, Monte-Carlo, designing to specifications, and optimization through component parameterization.

Simulation and Analysis with OCEAN: In this course, you explore ways to use OCEAN to run analog and mixed-signal simulations and manipulate your simulation results.

Virtuoso Spectre Circuit Simulator: In this course, you use the Spectre simulator from the command line to create netlists, compose scripts and run complex simulations

Using Virtuoso Spectre Simulator Effectively: This course teaches an in-depth look at the workings of the Spectre Circuit Simulator. You will learn the DC & AC analysis algorithms used by the simulator and the properties that affect the simulation.

RF Analysis with Virtuoso Spectre Circuit Simulator: This course teaches the RF Simulation Option. You set up, simulate, and analyze RF applications more quickly and more efficiently, running periodic steady state (PSS) analysis, small-signal analysis, and quasi-periodic steady state (QPSS) analysis among other advanced analyses.

Virtuoso UltraSim Full-Chip Simulator: In this course, you learn how to use the UltraSim Fast-SPICE simulator to run large transistor-based simulations, including an extensive set of checking commands, power analyses, and IR drop and electromigration tests.

Virtuoso AMS Designer: In this course, you learn to run and debug large and complex mixed-signal, mixed-language simulations from both the command-line and GUI using Verilog, Verilog-A, Verilog-AMS, VHDL, VHDL-AMS, Schematic, and Spectre and SPICE design blocks in mixed configurations.

Behavioral Modeling with Verilog or VHDL-AMS: These courses provide an in-depth approach to writing realistic behavioral models of analog and mixed-signal design blocks and systems using the respective modeling language.

Analog Modeling with Verilog-A: In this course, you will use the Virtuoso Analog Design Environment and Virtuoso Spectre Circuit Simulator to simulate analog circuits using Verilog-A models. You will use Verilog-A to model and design an analog-to-digital converter (ADC) and parts of a phase-locked loop (PLL), among other cells.

Analog Modeling and Simulation with SPICE by Andrei Vladimirescu: This course helps circuit designers better understand semiconductor device modeling, with an emphasis on deep-submicron (DSM) technology, and the operation of a SPICE circuit simulator. The course also addresses the different levels of modeling (structural and behavioral), simulation controls available to the user, and new types of analysis such as steady-state that are particularly suited for RF design.

Virtuoso Analog Design Update: This update training course introduces the new analog design features, graphical user interface, and use models based on the IC 6.1 Virtuoso platform. This course is designed for analog designers already familiar with previous versions of the Virtuoso platform, such as IC 5.1.4.1 and moving now to the new platform. This does not cover the migration steps.

Physical Design

Virtuoso Layout Design Basics: This course covers the basic techniques for working with designs in the Virtuoso Layout Suite L environment. You will learn to create and edit cell-level designs and to create and place instances to build hierarchy for custom physical designs.

Virtuoso Connectivity-Driven Layout: In this course, you will use example IC layouts to explore schematic-driven layout techniques. Virtuoso Layout Suite XL provides many features and automation improvements to assist you.

Virtuoso Space-Based Router: This course covers the Virtuoso Space-Based Router (VSR), which runs within the Virtuoso Layout Suite GXL environment. Block and chip level routing solutions can be quickly captured and managed using the Process Rules Editor (PRE) as well as customized Tcl scripts.

Virtuoso Chip-Assembly Router: This course covers the Virtuoso Chip-Assembly Router (VCAR), which provides flexible design constrained routing for device- and chip-level circuits.

Virtuoso Layout Migrate: This course covers process and design-rule migration of layout designs. You will also use preferred rules to improve yield and performance

Virtuoso Floorplanner: In this course, you will use the floorplanner to calculate the area needed for the top-level boundary and blocks. You will place the I/O pads, generate and place the top-level blocks, and complete a top-level floorplan.

Cadence Physical Verification System (PVS): This course covers practical methods of running and debugging DRC, ERC, and LVS. Users will learn how to use the powerful and straightforward PVS debugging environment to locate errors and fix real problems quickly.

Virtuoso Physical Design Update: This update training course introduces the new layout design features, graphical user interface, and use models based on the IC 6.1 Virtuoso platform. This course is designed for layout designers

already familiar with previous versions of the Virtuoso platform, such as IC 5.1.4.1 and moving now to the new platform. This does not cover the migration steps.

Infrastructure

Virtuoso Design Environment Setup: This streamlined course focuses on installing the Virtuoso Design Environment software, managing licenses, and troubleshooting file-locking issues.

Virtuoso Design Environment: This course covers the Virtuoso Design Environment administration, which includes installing the software, managing licenses, using Process Design Kits, customizing the environment, troubleshooting file-locking issues, and using SKILL commands.

SKILL Language Programming: This course provides the foundation, concepts, and sample programs to build SKILL programs.

SKILL Programming for IC Layout Design: This course provides a focused exploration of SKILL programming in the Virtuoso layout environment. You explore and enhance SKILL programs, which automate layout design tasks.

SKILL Development of Parameterized Cells: This course describes the tools and methods of developing parameterized cells (pcells) in SKILL. Pcells are the building blocks needed to leverage the connectivity-driven design environment for productivity gains.

Advanced SKILL Language Programming: This course focuses on the lexical scoping and object-oriented extensions to the SKILL language known as the SKILL++ language.

Verification

Assura Rules Writer: You will write and optimize rules for the Assura physical verification.

Cadence Assura® Verification: This course covers all aspects of using the Assura DRC and Assura LVS tools for design rule checks, short location, and layout versus schematic checks

Cadence QRC User Transistor-Level Extraction: This course covers Cadence QRC transistor-level parasitic extraction for analog and full-custom circuits.

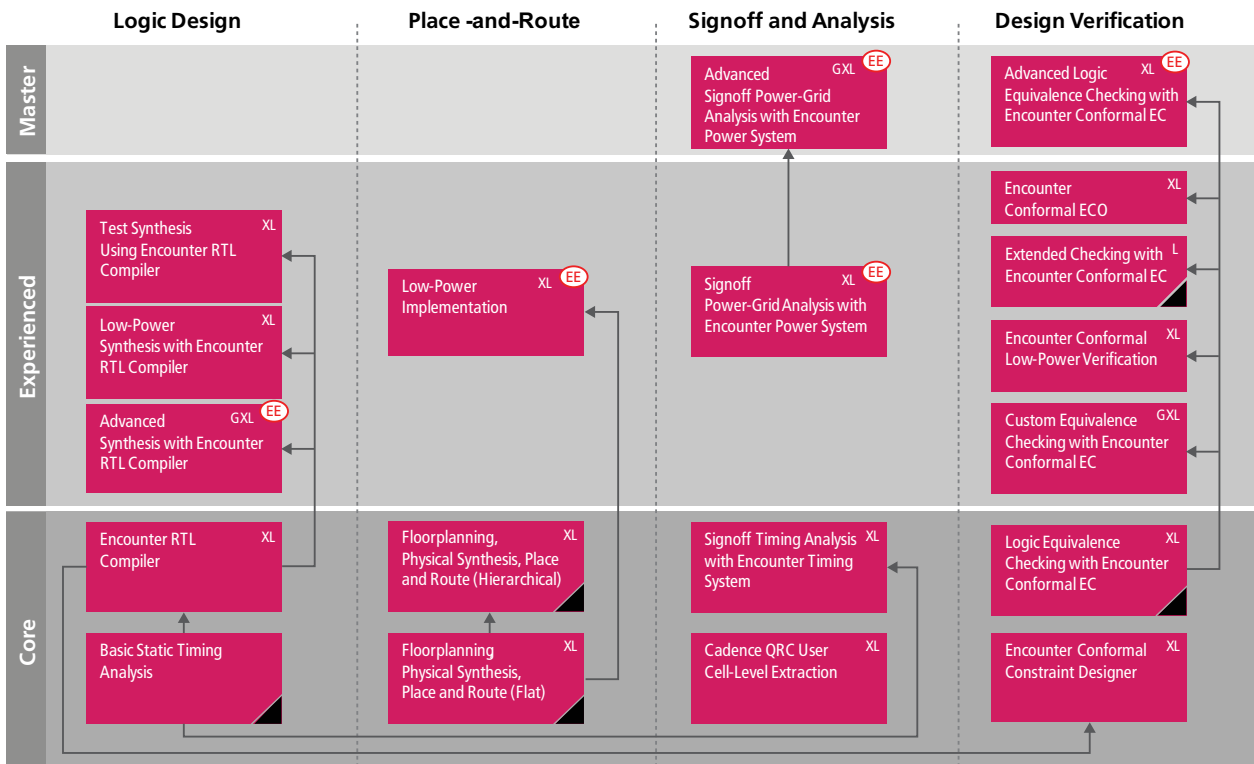
Cadence QRC Techgen Developer: This course begins with an overview of parasitic extraction, then uses existing RCX or QX technology files to create a technology file for the new QRC extractor.

MaskCompose Automated Reticle Design Synthesis: In this course, you will define a flow and process, build a reticle layout, produce documentation, generate a wafer layout, and use techniques that accelerate the design-to-manufacturing process.

Digital Implementation

Virtuoso Digital Implementation: This product consists of capacity-limited versions of Encounter RTL Compiler with global synthesis technology and the SoC Encounter L netlist-to-GDSII system. You will run the Virtuoso Digital Implementation system to synthesize an RTL netlist.

Learning Map



▲ Also available as an Internet Learning Series course. (EE) Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Some course titles may vary. Please refer to your regional catalog for exact titles & course datasheets.

Course Descriptions

Logic Design

Basic Static Timing Analysis: in this course, you learn the basic concepts of static timing analysis and apply them to constrain a design.

Encounter RTL Compiler: in this course, you explore the features of the Cadence® Encounter® RTL Compiler with global synthesis technology. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, optimize for low power, and interface with other tools.

Advanced Synthesis with Encounter RTL Compiler: In this course, you use Encounter RTL Compiler global synthesis to debug problems in the synthesis of complex designs when optimizing for timing, area, and power.

Low Power Synthesis with Encounter RTL Compiler: In this course, you use Encounter RTL Compiler with global synthesis to lower power consumption through single-pass multi-Vth optimization, hierarchical and multistage clock gating, multi-supply voltage (MSV) support, power shutoff, and state-retention power gating.

Test Synthesis using Encounter RTL Compiler: In this course, you learn to use Encounter RTL Compiler to insert test structures in your design, synthesize for test, and connect scan chains.

Place and Route

Floorplanning, Physical Synthesis, Place and Route (Flat): In this course, you explore high-level design planning and implementation by using the Encounter Digital Implementation (EDI) software. You will learn several techniques for floorplanning, placement, detail routing, and optimization while implementing timing closure strategies.

Floorplanning, Physical Synthesis, Place and Route (Hierarchical): In this course, you explore the features of the EDI software for creating and implementing a hierarchical design.

Low Power Implementation: In this course, you synthesize and implement several low-power techniques to reduce both dynamic and leakage power during logic synthesis implementation.

Signoff and Analysis

Signoff Timing Analysis with Encounter Timing System

System: This course is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Encounter Timing System (TS).

Cadence QRC User Cell-Level Extraction: In this introductory course, you explore parasitic extraction for standard-cell logic blocks in digital design.

Signoff Power-grid Analysis with Encounter Power System

System: In this course, you explore the need for power-rail analysis and use the Encounter Power System power consumption and power rail verification software to run several types of power-consumption and power-rail analyses.

Advanced Signoff Power-grid Analysis with Encounter Power System

System: In this course, you learn advanced features of the Encounter Power System including advanced library generation, Common Power Format (CPF) usage, power-up analysis, and thermal analysis.

Design Verification

Encounter Conformal Constraint Designer: In this course, you use Encounter Conformal® Constraint Designer to manage constraints for complex system-on-a-chip designs from RTL through layout.

Logic Equivalence Checking with Encounter Conformal EC

EC: In this course, you use the Encounter Conformal Equivalence Checker to perform functional verification. You learn the basic flow of equivalence checking and how to run hierarchical comparison of designs.

Custom Equivalence Checking with Encounter Conformal EC

EC: In this course, you run equivalency checks between the RTL and the abstracted logic design or abstracted memory circuits.

Encounter Conformal Low-Power Verification:

In this course, you learn to verify low-power designs using Encounter Conformal Low Power.

Extended Checking with Encounter Conformal EC:

In this course, you run clock-domain crossing (CDC) checks, semantic checks, and static property checks using the Encounter Conformal Equivalence Checker tool.

Encounter Conformal ECO:

In this course, you learn how to implement functional ECO analysis and generation, design netlist modification, clock domain synchronization, and semantics checks by using the Cadence Encounter Conformal ECO Designer tool.

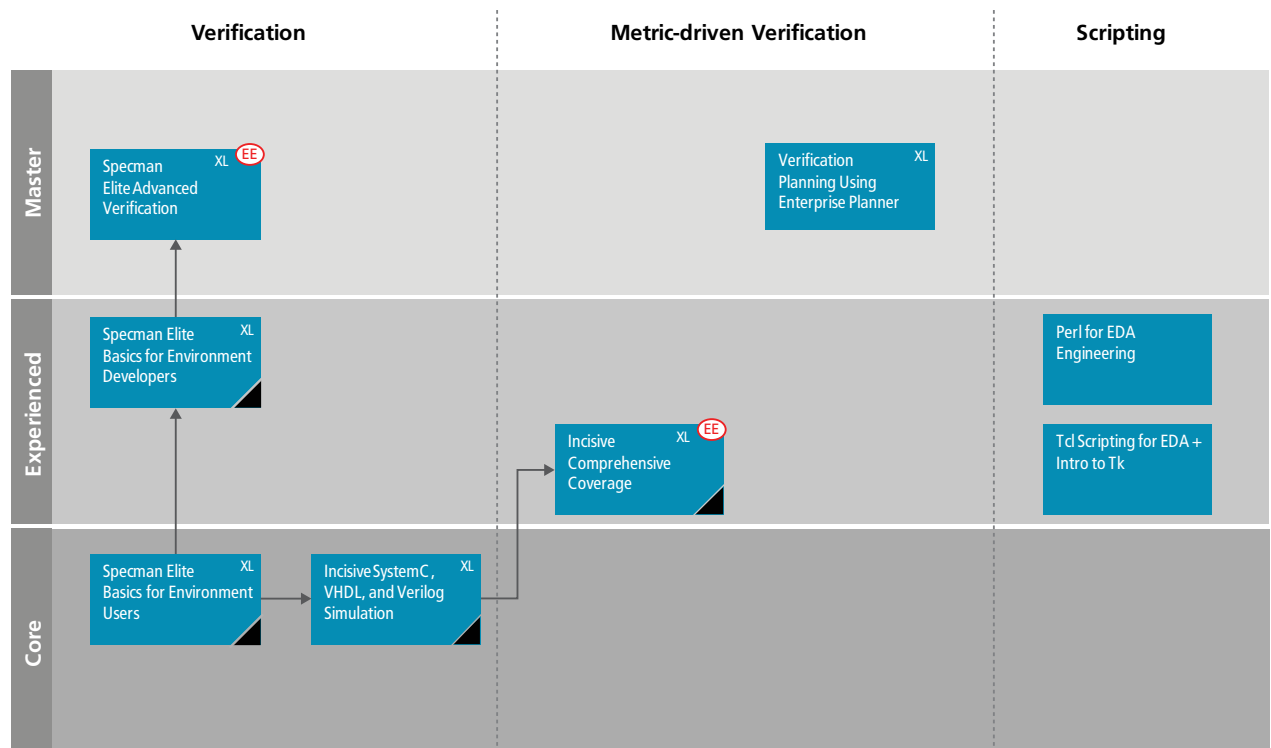
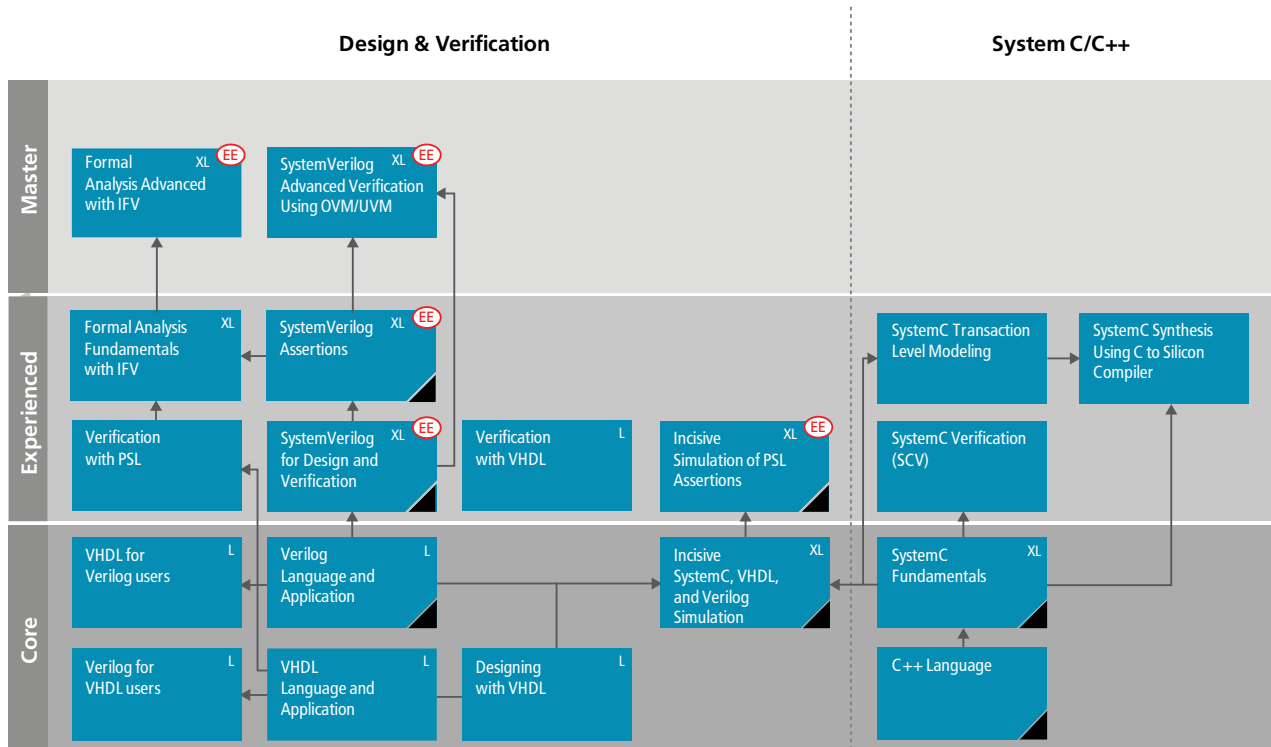
Advanced Logic Equivalence Checking with Encounter Conformal EC

EC: In this course, you learn systematic procedures for diagnosing the nonequivalences caused by setup, modeling, and mapping issues.



DIGITAL VERIFICATION, LANGUAGES, AND METHODOLOGIES WITH INCISIVE TECHNOLOGY

Learning Maps



▲ Also available as an Internet Learning Series course. (EE) Denotes Advance with Engineer Explorer class. L, XL, GXL Denotes tiers of Cadence products used in course. Some course titles may vary. Please refer to your regional catalog for exact titles & course datasheets.

Course Descriptions

Verilog® Language and Application: A worldwide industry standard, the course provides a thorough background in the use and application of Verilog for digital hardware design.

VHDL Language and Application: The course provides a thorough background in the use and application of VHDL—A worldwide industry standard—to digital hardware design.

Verification with VHDL: As ASIC and FPGA designs grow in complexity, verification is becoming the greatest challenge for completing design projects on time. To address this challenge, designers must make the most of VHDL's capabilities, as well as adopting verification techniques such as Transaction-Level Modeling (TLM) and Assertion Based Verification (ABV).

Formal Analysis Fundamentals with Incisive Formal Verifier: This course introduces the principles of Formal Analysis (FA) and provides techniques for making the most effective use of a Formal Analysis tool.

Formal Analysis Advanced with Incisive Formal Verifier: This advanced course examines complex Formal Analysis methodology and tool features, including links to verification planning and management that complement simulation strategies.

Verification with PSL: This course provides a deep introduction to PSL, followed by guidelines and methodologies for describing and debugging complex design properties.

SystemVerilog

SystemVerilog for Design and Verification: This course gives an in-depth introduction to the main enhancements of SystemVerilog, discusses the new features, and demonstrates how design and verification is more efficient and effective when using SystemVerilog constructs.

SystemVerilog Assertions: This course gives you an in-depth introduction to SVA, together with guidelines and methodologies to help you create, manage, and debug effective assertions for complex design properties.

SystemVerilog Advanced Verification using OVM/UVM: This course examines the construction of verification components based upon the OVM library to develop powerful, reusable, and robust verification environments.

Simulation and Coverage

Incisive SystemC, VHDL, and Verilog Simulation: This short course thoroughly explores compilation, elaboration, and simulation using Incisive. The course treats VHDL, Verilog, and SystemC equivalently; students may do most labs in their choice of language.

Incisive Comprehensive Coverage: This course introduces the Incisive comprehensive coverage features that measure how thoroughly your testbench exercises your design.

Incisive Simulation of PSL Assertions: This course teaches the basics of assertion-based verification using the PSL language in simulation. Focus is given to making use of property checking in simulation and using Simvision and coverage to check the results of your assertions.

SystemC/C++

C++ Language: This course begins with Essential C++ for SystemC, covering all C++ language features essential for an understanding of SystemC, including classes, inheritance, virtual functions, templates, and late binding.

SystemC Fundamentals: This course teaches the fundamentals of SystemC, describes the features of the language, and explores how it can be used for system, hardware, and verification modeling.

SystemC Verification: This course describes the background to advanced verification techniques such as Transaction-Level Modeling, randomization, and dynamic resource generation.

SystemC Transaction-Level Modeling (TLM): This course builds on your knowledge of the SystemC language, covering the newly provided APIs and the modeling methods used to implement TLM-based systems.

SystemC Synthesis Using C-to-Silicon Compiler: This course provides what a designer needs for high-level synthesis, from coding SystemC for synthesis, to using the tool to generate optimized designs.

Specman Verification

Specman Elite Basic for Environment Users: This course introduces the foundation of the *e* language and teaches how to effectively use a verification environment.

Specman Elite Basic for Environment Developers: This course teaches how to create a modular, reusable verification environment using the *e* language. The course is based on a metric-driven verification methodology that is applicable to a broad range of designs.

Specman Elite Advanced Verification: This advanced course examines the use of advanced *e* language features to develop reusable and scalable verification environments.

Metric-Driven Verification

Verification Planning using Enterprise Planner: This course teaches how to build a verification plan using Enterprise Planner giving special attention to the planning process and the need for rigorous planning. All aspects of Enterprise Planner are discussed.

Scripting

Tcl scripting for EDA + Intro to Tk: This compact course is the fastest and most effective method for engineers to understand the potential of Tcl and become proficient in the language; Tk part teaches fundamental concepts like how to create widgets, how to lay them out, and how to “bind” new behaviors to events.

Perl for EDA Engineering: This course was written from the ground up with EDA professionals in mind. It teaches both basic and advanced concepts of Perl for processing large volumes of data, translating tool output formats, and assisting in general shell and tool tasks. This course is invaluable to anyone working with Perl scripts on a regular basis.

METHODOLOGY-BASED LANGUAGE TRAINING

HDL Language

- Verilog Language and Application
- VHDL Language and Application

SystemVerilog

- SystemVerilog Design and Verification
- SystemVerilog Assertions (SVA)
- Advanced Verification using OVM/UVM

SystemC

- C++/SystemC Fundamentals
- SystemC Transaction Level Modeling (TLM) *NEW*
- SystemC Synthesis Using C-to-Silicon Compiler *NEW*

Specman

- Specman Elite for Verification Environment Users
- Specman Elite for Verification Environment Developers
- Specman Elite Advanced Verification

Verification

- Verification with PSL
- Formal Analysis Fundamentals and Advanced with Incisive Formal Verifier *NEW*

Script

- Perl for EDA Engineering *NEW*
- Tcl Scripting for EDA/Introduction to Tk



Reference Guides are available upon request

PROMOTIONAL OFFER

Register and attend the following methodology-based language training courses and receive a complimentary book voucher*

- SystemVerilog Assertions (SVA)
- Advanced Verification using OVM/UVM
- SystemC Synthesis Using C-to-Silicon Compiler *NEW*
- Specman Elite Advanced Verification
- Formal Analysis Fundamentals and Advanced with Incisive Formal Verifier *NEW*
- Perl for EDA Engineering *NEW*

* Offer valid on new registrations. Not to be combined with other promotions or discounts. The book voucher is valued at US \$25/EUR 25€. This offer is valid until December 31st, 2010, while stock lasts. Register using promo code: Brochure2010.

WORLDWIDE LEADERS IN METHODOLOGY-BASED LANGUAGE TRAINING FOR ELECTRONIC DESIGN

- Education is our sole mission. This focus and commitment has allowed us to develop a style of training that gives you the best possible return on your investment with us.
- We Offer a Variety of Industry-renowned Classes on Languages and Methodologies.
- Design, Verification, Assertion and Scripting languages such as SystemVerilog, OVM, VHDL, SystemC, TLM, C-to-Silicon Compiler, Specman *e*, Perl, and Tcl.

WHAT SETS US APART FROM OTHER TRAINING PROVIDERS

- Expert developers, experienced trainers
- High-quality, standards-based content
- Open-minded, flexible approach
- Innovative, up-to-date course materials
- The latest remote learning options
- World-wide training centers

Find out more at
www.cadence.com/training/eu/
or www.esperan.com

TESTIMONIALS

SystemVerilog Design and Verification

“A real eye-opener for this old-school Verilog designer”

SystemVerilog Assertions

“Much more efficient (and enjoyable) than trying to learn this stuff from a textbook”

Verification with VHDL

“Valuable verification concepts, examples, and ... suggestions, combined with good open discussion”

© 2010 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, 1st Silicon Success, Accelerating Mixed Signal Design, Allegro, Assura, BuildGates, Conformal, Concept, Connections, Diva, Dracula, ElectronStorm, Encounter, EU CAD, Fire & Ice, First Encounter, HDL-ICE, Incisive, Invisible Specman, IP Gallery, InstallScape, NanoRoute, NC-Verilog, NeoCell, NeoCircuit, Neo Circuit—RF, NeoIP, OpenBook, OrCAD, OrCAD Capture, OrCAD Layout, Palladium, Pearl, PowerSuite, PSpice, SignalStorm, Silicon Design Chain, Silicon Ensemble, Silicon Express, SKILL, SoC Encounter, SPECCTRA, SPECCTRAQuest, Spectre, Specman, Specman Elite, SpeedBridge, Verilog, Virtuoso, VoltageStorm, and Xtreme are either trademarks or registered trademarks of Cadence Design Systems, Inc. in the United States and/or other jurisdiction. Esperan is a Cadence company. OSCI, SystemC, Open SystemC, and Open SystemC Initiative are registered trademarks of Open SystemC Initiative, Inc. in the United States and other countries and are used with permission. All other trademarks are the property of their respective holders.

21538 07/10 MK/DM/Print

TRAINING LOCATIONS

NORTH AMERICA

Arizona

Cadence Design Systems, Inc.
1620 W. Fountainhead Pkwy, Suite 219
Tempe, AZ 85282

Location Tel: (480) 413-9550
Registration Tel: (800) 787-2460

training_enroll@cadence.com

California

Cadence Design Systems, Inc.
2655 Seely Avenue, Bldg. 6
San Jose, CA 95134

Location Tel: (408) 944-7654
Registration Tel: (800) 787-2460

training_enroll@cadence.com

Texas

Cadence Design Systems, Inc.
12515-7 Research Boulevard, Suite 250
Austin, TX 78759

Location Tel: (512) 349-1100
Registration Tel: (800) 787-2460

training_enroll@cadence.com

Massachusetts

Cadence Design Systems, Inc.
270 Billerica Road
Chelmsford, MA 01824

Location Tel: (978) 262-6584
Registration Tel: (800) 787-2460

training_enroll@cadence.com

Ottawa, Ontario

Cadence Design Systems LTD
1130 Morrison Drive, Suite 240
Ottawa, ON Canada K2H 9N6

Location Tel: (613) 828-5626
Registration Tel: (800) 787-2460

training_enroll@cadence.com

EMEA

France

Cadence Design Systems S.A.S.
Bâtiment Avenir
18, rue Grange Dame Rose - BP 128
78148 Vélizy Cedex
France

Tel: +33 (0)1 34 88 53 48/54
Fax: +33 (0)1 34 88 53 01

training_france@cadence.com

Germany

Cadence Design Systems GmbH
Mozartstrasse 2
85622 Feldkirchen (München)
Germany

Tel: +49 (0)89 4563 19 60 / 61 / 62
Fax: +49 (0)89 4563 1919

training_germany@cadence.com

Israel

Cadence Design Systems (Israel) Ltd
6 Hahoshlim St., PO Box 2187
Life Plaza, Building C
Herzeliya, 46121

Tel : +972 (0) 9 971 2551
Fax: +972 (0) 3 760 4683

training_israel@cadence.com

Italy

Cadence Design Systems S.r.l.
Milanofiori-Strada 7
Palazzo R/3
20089 Rozzano, Milano
Italy

Tel: +33 1 34 88 53 48/54
Fax: +33 1 34 88 53 01

training_italy@cadence.com

Sweden

Cadence Design Systems AB
Isafjordsgatan 30C
S-164 40 Kista
Sweden

Tel: +44 (0)1 344 866 539
Fax: +44 (0)1 344 865 347

training_uk@cadence.com

United Kingdom

Cadence Design Systems Ltd
Bagshot Road
Bracknell
Berkshire RG12 0PH
England

Tel: +44 (0)1 344 866 539
Fax: +44 (0)1 344 865 347

training_uk@cadence.com

INDIA

Cadence Design Systems India Pvt Ltd
Building 3B, 2nd Floor, RMZ Ecospace
Sarjapur Outer Ring Road
Bangalore 560 103

Tel: +91-80-4184 1111
Fax: +91-80-4184 1122

India_es@cadence.com

CHINA

Cadence Design Systems
suite 06-08 in 1101 of 11th floor, suite
1201 of 12th floor, and suite 0108 in
1501 of 15th floor,
Metropolis Tower ,No.2 Dong San Str.,
Haidian District, Beijing,
100080 P.R China

Tel: +86-21-6122-2389
Fax: +86-21-6288-2602

training_china@cadence.com

Cadence Design Systems
Room 1801, Headquarters Building
168 Middle Xi Zang Road, Shanghai
200001, P.R. China

Tel: +86-21-6122-2389
Fax: +86-21-6288-2602

training_china@cadence.com

JAPAN

Cadence Design Systems, Japan
2-100-45 Shin-Yokohama, Kohoku-ku
Yokohama 222-0033 Japan

Tel: 045-475-2619
Fax: 045-474-9435

japan_esg@cadence.com
[http://www.cadence.co.jp/training/
training_index.html](http://www.cadence.co.jp/training/training_index.html)

KOREA

Cadence Design Systems, Inc.
6Fl., KPS Building 196 Keumgok-Dong,
Bundang-Gu Sungnam-Si,
Kyunggi-Do 463-726 Korea

Tel: +82-31-728-3036
Fax: +82-31-728-3037

training_korea@cadence.com

SINGAPORE

Cadence Design Systems, Inc.
1 International Business Park
#04-11 The Synergy
Singapore 609917

Tel: +65-6895-5151
Fax: +65-6569-0688

training_singapore@cadence.com

TAIWAN

Cadence Design Systems, Inc.
3F No. 28 Industry E. 9th Road
Science-Based Industrial Park,
Hsin-chu 300, Taiwan R.O.C.

Tel: +886-3-566-3852
Fax: +886-3-578-0422

nicolew@cadence.com