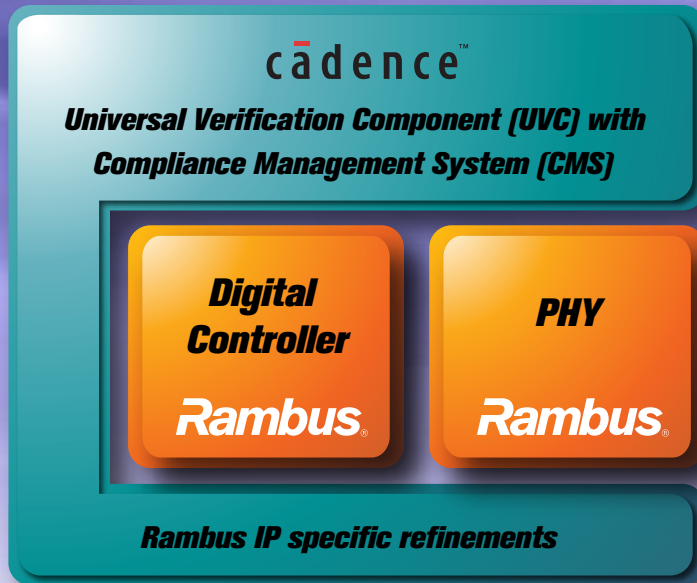


Rambus[®] cādence™

PCI Express Design and Verification IP Integration

Technical Brief



OVERVIEW

Best-of-Breed design and verification IP integrated solution

Design IP independently verified using Cadence VIP Automated Protocol Compliance Management System (CMS), customized specifically for Rambus IP

Highest quality solution minimizing verification time and protocol expertise required

BENEFITS

Easy integration through highly adaptable interfaces

Push-button verification for 70+% coverage without writing tests

Superior design IP and verification IP integration shortening time to market

Minimized integration and bring up time and reduced protocol expertise required

Highly Configurable. Superior Architecture. Independently Validated.

Superior Design IP and Verification IP Integration

One of the key characteristics of SOC design today is the need to reuse Intellectual Property blocks to implement standard functions or protocols. The use of IP blocks can save time and effort but comes with its own set of risks that must be managed. First there is the issue of finding a high quality IP vendor to supply the needed function, then once the IP is selected, there is a need to verify the IP integration within your design.

Integrating the "Best-Of-Breed" Digital controllers and PHYs from Rambus with Verification IP from Cadence as an integrated solution, provides customers with a predictable, independently cross-checked solution for PCI Express.

Rambus Gen 2 Digital Controller Family: An Enhanced Architecture

The Rambus[®] Gen2 Digital Controllers are a family of products for implementing the Transaction, Data Link, and MAC Layers of high-speed serial links. Rambus' Gen2 controllers represent a second-generation architecture, carefully designed for easy integration via adaptable interfaces. These controllers also optimize link utilization and

are customizable for performance, power consumption, and silicon footprint targets. The Rambus Digital Controllers are available in switch port, crossbar switch, end point, root complex, or hybrid (endpoint and root complex) elements. They are simple, configurable, and layered architectures, independent of application logic, implementation tools, and target technology. Rambus' Digital Controllers provide highly scalable bandwidth through configurable link width, data path width, and clock frequency. This optimizable solution is ideal for a wide range of applications ranging from low-power mobile applications to high performance graphics solutions demanding full high-bandwidth PCI Express[®] protocol implementation.

Ease of Chip Level Integration

Rambus offers optional tools and IP to make system integration quick and effective. Rambus provides PCI Express-to-AXI and PCI Express-to-AHB bridges that connect industry-standard buses directly to the Rambus Digital Controller. This tool enables quick integration onto SoC onchip buses. Rambus also offers performance specific interfaces for connecting application logic directly to the PCI Express stack, specifically designed to meet the system's interface, bandwidth and latency requirements.

Rambus Digital Controllers are also independent of the target technology. As a result, customers are able to easily migrate among COT, FPGA, gate array, structured ASICs, and standard cell technologies for early testing as well as volume production implementation.

Independently Verified Solution

Rambus Digital Controllers are uniquely cross-verified using Cadence's Verification IP as well as an internal test suite. This ensures that verification is performed independently, and tight integration with the verification IP is also ensured.

Interoperable with PCI Express PHYs

Rambus PHY cells support the PCI Express Physical Layer through the PIPE interface. To complement the Digital Controllers, Rambus provides a robust Gen2 PHY solution with streamlined footprint and low-power dissipation as well as feature-rich in-system diagnostics and testability for high yield production. The customer can, alternatively, choose to implement a customized PHY and seamlessly attach it to the Rambus Digital Controllers through the standardized 8-, 16-, or 32-bit PIPE interface.

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Rambus Specific Refinements

Compliance Management System

Compliance vPlan

Compliance Coverage and Metrics

Compliance Reporting

Compliance Test Suite

Cadence PCI Express Verification IP

Benefits

- Maximizes quality with complete, easy to use protocol compliance verification
- Maximizes productivity by automating management of compliance verification to closure
- Ensures clear status communications within engineering team
- Most efficiently achieves compliance verification closure with unique automated PCI Express Compliance Management System (CMS)
- Delivers greatest predictability and team communications using metrics based compliance measurement and reporting

Universal Verification Component (UVC)

UVCs are testbench Verification IP that provide a powerful simulated verification environment for block and system-level verification. Only UVCs provide you the choice of using SystemVerilog and/or e for your testbench. They provide automatic stimulus generation, assertion checking, and functional coverage analysis all within a configurable, extensible, highly reusable product. Better yet, each UVC now includes the industry's most automated compliance solution called the Compliance Management System (CMS). CMS greatly simplifies and automates verification by achieving 70+% coverage without the need to write tests.

Supports Verification For			
Protocol Version	End Point	Root Complex	Switch
Gen1	✓	✓	✓
Gen2	✓	✓	✓

UVCs offer the most flexibility and control over stimulus generation ranging from fully random to fully directed testing. The UVC includes a powerful sequence generator that automatically creates all types of PCI Express transactions, including error packets. It provides data and assertion checking, and it performs functional

coverage analysis using a fully integrated coverage model.

Additionally, since UVCs are all built based on the Incisive Plan to Closure Methodology (IPCM) they can be reused throughout the verification process without expending any extra effort. You'll fully retain your investment when moving from module- to block- to system-level verification or when verifying derivative products.

Automated Compliance Management System

Key to the PCI Express UVC's ability to automate compliance verification is the unique Compliance Management System (CMS). CMS consists of a Compliance Verification Plan (vPlan), Compliance Test Suite, compliance metrics, and a compliance coverage model. The user only interacts with the vPlan and the test suite while CMS manages all of the data "under the hood". This enables you to achieve compliance more productively and more predictably. CMS also saves time and reduces the degree of protocol expertise required. With the integrated PCI Express solution Rambus provides IP specific CMS refinements. These refinements enable even greater levels of coverage to be automatically achieved over and above the standard PCI Express CMS.

Rambus

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